IN THE SPECIFICATION:

Please amend the paragraph beginning on page 19, line 20 to read as follows:

In the embodiments shown, the critical path starts at the C_{in} input and traces through AND-OR-INVERT gate 309, INVERT-AND-GATE 317, and AND-OR-INVERT gate 431~~, and INVERT-AND-GATE 317~~. In these embodiments, the elements on the critical path are buffered from the rest of the circuit to minimize the load on the critical path and therefore increase the speed of the critical path. For example, the carry outputs $C_{1\text{-}11}$ are buffered from the critical path by two or more buffers, thus isolating the critical path from the carry generates $C_{1\text{-}11}$. In particular, the output of AND-OR-INVERT gate 309 is routed through buffers 310 and 311 before it is provided to Final XNOR block 161. In addition, intermediate generate gates, intermediate propagate gates, and intermediate carrys are buffered from the critical path to minimize the load on the critical path. According to embodiments of the invention, a signal that is inverted by such a buffer may be reinverted by the gate that is receiving the signal. Thus, for example, the signal that is input to INVERT-AND-OR gate 317 is logically inverted prior to performing the AND-OR function. By contrast, the critical path proceeds from one complex gate to another without any buffers or other inversion. In an embodiment, most of the capacitance being driven by gate 317 is capacitance from gate 431 of FIG. 4.

Please amend the paragraph beginning on page 21, line 19 to read as follows:

This embodiment contains a number of transistor stacks which are connections from a voltage supply to an output. One stack in AND-OR-INVERT gate 431 is transistor 701 and transistor 702 (to output ~~701~~710). Another is transistor 701 to 705, and another is transistor 704 to 703. In an embodiment, the

stacks are tapped so that the transistor closer to the output is smaller. For example, transistor 701 may be 2.6 microns, transistor ~~701~~ 702 may be 1.3 microns, and transistor ~~701~~ 705 may be 1.3 microns. As another example, transistor 704 may be 2 microns and transistor 703 may be 1 micron. Transistor 706 may be .7 microns. In this example, the PMOS transistors may be sized larger than the NMOS because of lower mobility. As discussed above, the use of the tapered stack may allow for an increase in speed in the critical path, which includes transistors 702 and 703, in that the larger transistor has reduced resistance and thus a reduced delay. In this way, the load on the critical path may be reduced. In an embodiment, the delay of AND-OR-INVERT gate 431 may be reduced to about the delay of an inverter with a fanout of 2. The use of the tapered stack may provide for crisper edge rates on the output because of the increased speed, which may tend to create higher edge rates for succeeding stage. In an embodiment, every transistor stack in the critical path of adder 100 is tapered. In another embodiment, every transistor stack in adder 100 is tapered.